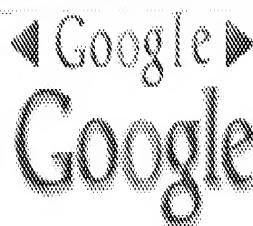


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instruction simulator includes. **Memory/Register** dump. Breakpoint setting. Running program. Step **execution**. Show statistics such as number of **instructions** ...

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data **dependency** or resource **conflict** is found. Issued. **instructions** To implement this **out-of-order execution** control, the. **register** lock bits, pipeline ...

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an update to a **register** or **memory** location by one **instruction** may not be detected by an must be stalled due to resource **conflicts** or data **dependencies** ...

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of-order execution, register renaming, and many forms of caching [HP96]. **instructions** must be stalled due to resource **conflicts** or data **dependencies** ...

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The arc represents the **dependency** concerning the **order of execution** **instruction** between **register** and **memory**, and. (3) is the **instruction** for the ...

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7. Simulation/evaluation environment for a VLIW processor architecture

Aggressive in-order wide-issue **execution** leads to very long **instruction** word (VLIW) dealing with issues such as **register dependencies** and operation ...

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and only the Load and Store **instructions** can access **memory**, with respect to a base processor. (single-cycle, non-pipelined, in-order **execution** model) [13]. ...

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In **order** to show that the sequential **execution** of each **instruction** is correctly cessor or to the contents of the data **memory**. Such data **dependencies** ...

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True operand **dependencies**, rather than program **instruction order**, largely determine The major blocks in the **execution** core are the **register file** , ...

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I/O. Other scripts were used to **compare** the **simulation** result against a golden this function can load content of a **file** to the **memory**. **SAVE_MEM**, ...

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1.9.6.1 Change contents of any **memory** address prior to **simulation** run ... Makes it possible to **dump** binary traces of internal signal activity to a **file** for ...

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simulation was stored as a reference **file**, and **files** resulting instructions between **register dumps**, errors might be masked ...

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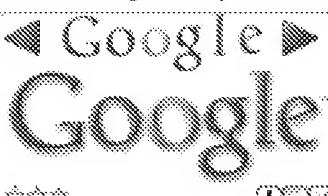
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exercising the **processor** to its **design** limits and thereby. exposing bugs that would not be readily detected using. simulation-based **verification** techniques. ...

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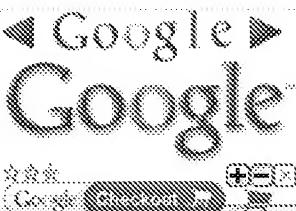
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cache **verification** means fails ... is capable of executing an instruction for any ...

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DB Rutherford Jr - US Patent 4,740,972, 1988 - [freepatentsonline.com](#)

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F Corella, Z Zhou, X Song, M Langevin, E Cerny - Formal Methods in System Design, 1997 - Springer

... that ROBDD-based **verification** methods often take too long, or run out of **memory**, when applied to ... In this case the CPU time needed for **verification** is of ...

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Method and apparatus for securing access to a computer facility

JR Michener - US Patent 4,802,217, 1989 - [Google Patents](#)

... computer system for **verification**. The security unit ... must have a non-volatile and inaccessible **memory**, a ... CPU (ie, microprocessor) and a standard "smart" ...

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[BOOK] Distributed Algorithms

NA Lynch - 1996 - [books.google.com](#)

... 23.4 Modelling Shared **Memory** and Network Systems 768 23.4.1 Shared **Memory** Systems

768 ... Synchrony 773 24.1 The Problem 773 24.2 A Single-**Register** Algorithm 774 ...

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Local area network bridge

MJ Leone - US Patent 4,922,503, 1990 - [freepatentsonline.com](#)

... circuit 109, which receives a **processor** clock input ... in order to provide a statistical

verification of the ... stored and located in global **memory**, how abbreviated ...

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Cable television radio frequency data processor

JC McMullan Jr, DJ Hoder, DR Huntley - US Patent 5,142,690, 1992 - freepatentsonline.com

... Security apparatus with alarm search and **verification** capability. ... control unit of the RF-IPPV **processor** also sorts ... be deleted from the RF-IPPV module **memory**. ...

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[CITATION] COMMERCE ELECTRONIQUE PAR RESEAU DE TRANSACTIONS

INC QPASS, M COCKRILL, W BRYANT, D FRANKLIN, M ... - WO Patent 33,221, 2000

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Memory management and protection system for virtual **memory** in computer system

H Nozue, M Saito, K Maeda, S Asano, T Okamoto, S ... - US Patent 5,890,189, 1999 - freepatentsonline.com

... of a special instruction on a **processor** side, an ... the address table entries, when the **verification** means verifies ... space realized by the **memory** protection device ...

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Tokenless biometric electronic financial transactions via a third party identicator

PD Lapsley, JA Lee, DF Pare, N Hoffman - US Patent App. 09/731,536, 2000 - Google Patents

... IDENTIFIER TO FINANCIAL TRANSACTION **PROCESSOR** 806 TRANSACTION ... because the comparison and **verification** process is ... any personalized man-made **memory** tokens such ...

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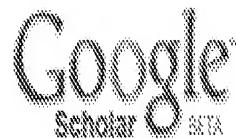
Key authors: [J McMullan](#) - [D Hoder](#) - [D Huntley](#) - [D Naddor](#) - [R Beyers](#)

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[A methodology for the verification of a "system on chip" - \[PDF\]](#) [sloca.org](#)

D Geist, G Biran, T Arons, M Slavkin, Y Nustov, M ... - Proceedings of the 36th ACM/IEEE conference on Design ... , 1999 - portal.acm.org

... on automatic generation of testcases and automatic checking of **simulation** results,

similar to methods used in **processor** and system **verification**[1, 2 ...

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[Realization of a programmable parallel DSP for high performance image processing applications - \[PDF\]](#) [acm.org](#)

JP Wittenburg, W Hinrichs, J Kneip, M Ohmacht, M ... - Annual ACM IEEE Design Automation Conference: Proceedings of ... , 1998 - doi.ieeecomputersociety.org

... Data from cycle true **simulation** of assembler coded programs ... al- gorithm cores on

the C++ **processor** model already ... important part of the later **verification** on RTL ...

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[Verification of instruction and data fetch resources in a functional model of a speculative out-of ...](#)

GS Averill - US Patent 5,805,470, 1998 - [freepatentsonline.com](#)

... devices connected to it except for **processor** 100 ... reduces the amount of total **simulation**

time required ... In addition, real-time **verification** reduces the amount of ...

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[\[BOOK\] Performance and Functional Verification of Microprocessors - \[PS\]](#) [ibm.com](#)

P Bose, JA Abraham - 1999 - IBM TJ Watson Research Center

... and J. Edmondson, "Performance **simulation** of an ... towards an integrated **processor**

validation methodology ... on microprocessor testing and **verification**, Sept./Ott. ...

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[RAPTOR: a single chip multiprocessor](#)

SW Lee, YS Song, SW Kim, HC Oh, WJ Hahn - ASICs, 1999. AP-ASIC'99. The First IEEE Asia Pacific ... , 1999 - [ieeexplore.ieee.org](#)

... This **simulation** environment allows the **verification** stimuli to ... the pseudorandom test

based **verification** method with ... of implementing the **processor** with current ...

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[Speculative execution of test patterns in a random test generator](#)

D Weir, RC Brockmann - US Patent 5,729,554, 1998 - [freepatentsonline.com](#)

... test generator 2 and can be used in the **verification** of a complex design such as a CPU. ... the current behavioral model state to the pre-**simulation** state in ...

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Verification of accesses in a functional model of a speculative out-of-order computer system

GS Averill · US Patent 5,815,688, 1998 · Google Patents

... BEHAVIORAL MODEL \ STATE ADVANCE **SIMULATOR** TO POINT ... present invention relates generally to **verification** methods for ... been developed to increase **processor** speeds ...

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A study on logic design and architecture simulator design of a newon-chip multiprocessor

WJ Hahn, K Park, SH Choi, SH Yoon - TENCON 99. Proceedings of the IEEE Region 10 Conference, 1999 · [ieeexplore.ieee.org](#)

... including 16Kbytes on-chip cache for each general **processor**. ... Figure 3. **Verification**

Model As shown in Figure 3, we built the **simulation** model by adding ...

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[BOOK] ATUM: a new technique for capturing address traces using microcode

A Agarwal, RL Sites, M Horowitz - 1986 - IEEE Computer Society Press Los Alamitos, CA, USA

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AE32000: an embedded microprocessor core

HC Oh, HG Kim, HS Jung, JW Lee, BJ Kim, JY Jung, ... - ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE ... , 2000 · [ieeexplore.ieee.org](#)

... as SPEC is used by workstation-**processor** vendors. ... LM.Noack., " I'm Done **Simulation**;

Now What ... **Verification** Coverage Analysis and Correctness Checking of the ...

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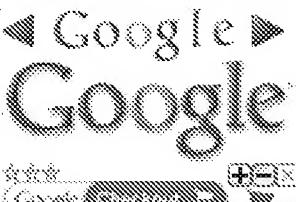
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model, a copy of **register file** contents to **memory**). At Finally, the **memory dump**. area **file** from the **simulation** was compared ...

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2. I'm Done Simulating; Now What? Verification Coverage Analysis and ...

Cache **Coherency** Checkers. 9%. Reference Model Comparison. **Register File** Trace Compare Fault **simulation** was not used for functional **verification** of the ...

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by M Kantrowitz - 1996 - Cited by 94 - Related articles - All 5 versions

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3. Verification of the UltraSPARCTM Microprocessor

during a regression, the value change **dump file**, along. with **simulation** logs, would be **memory** arrays (caches, **register files**, etc.) were imple- ...

doi.ieeecomputersociety.org/10.1109/CMPCON.1995.512422 - Similar pages

by S Mehta - 1995 - Cited by 13 - Related articles

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severe limitations on complete **verification** of a custom **memory** ... structures, **register files** and some custom datapath designs. Unlike. the **verification** ...

www.synopsys.com/products/esp/sun_ss.pdf - Similar pages

5. Whitepapers

Because they are unfamiliar with logic **simulation** and emulation tools, they pass **memory** image **files** to the **verification** engineers who run the test. ...

www.verisity.com/resources/whitepaper/hwswoverification.html - 60k - Cached - Similar pages

6. THE ACM COMPUTING CLASSIFICATION SYSTEM Copyright 1995 by ...

... models **Simulation Verification** Worst-case analysis B.4.5 Reliability, hierarchies Swapping Virtual **memory** D.4.3 **File** Systems Management (E.5) ...

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7. [PDF] Feldstein SPARC-V9 Simulator Version 1.0 Software Requirements ...

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verification may be performed at **simulation** time. Produces trace **files** of ... Run-time **coherency** monitor/protocol checker.

1.6.7.5.4.2 **Memory** and Cache ...

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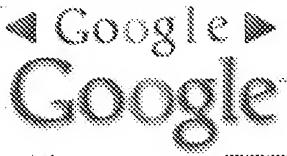
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embedded **memory models** used in RTLs) is designed. for **simulation** speed, and functional accuracy. **verification** tools to double-check the **consistency** of ...

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... **register** values, micro-operations and. **memory content** on the screen. The designers eradicate ... comparing the two **models'** **consistency** and obviated the ...

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by JS Yim - 1997 - Cited by 6 - [Related articles](#)

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CMV for the **verification** of C **model**. Co-**simulation** Environment. Polaris codes and **memory content** on the screen as shown. in Fig. 7. ...

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The majority of **verification** tests ran on these **models**. The terms hardware/ firmware (HW/FW) co-**simulation** and VPO imply that this activity begins ...

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6. [Using Term Rewriting Systems to Design and Verify Processors](#)

Thus, $rf[r]$ refers to the **content** of **register** r , and $rf[r := v]$ represents For example, elsewhere we have defined a new **memory model** and associated ...

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default **memory model**, our **simulator** implements Sequential **Consistency** as a correct implement of TSO. We **model**, a MOSI

directory protocol, similar to that ...

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from HCL to C to construct **simulation models** of the two processors, (C) requires **register consistency** within each stage as well as that ret ...

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9. Method and apparatus for creating a multiprocessor verification ...

The **simulation models** usually include one or more various subsystems, The system state may include the **register** contents, cache and **memory** contents ...

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10. Instruction-Set Simulation and Tracing

More modular hardware **simulator** interfaces that simplify the process of adding new processor, **memory** system, and device **models** ...

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